# LTspice Pulsed T-Line Lab

# Seth Ricks

# ECEN 390

Brother Swenson

**ECEN–390: LTspice Pulsed T-Line Lab (82 points)**

(jas, LTspice Pulsed T-Line Lab.docx, 5/20/2025)

**Note: This is a CAD lab to be done individually, rather than in teams, although please help each other out if/when opportunities arise, avoiding plagiarism. Submit an electronic version of a lab report to receive credit for doing this lab.** The goal of your **lab report is to provide sufficient documentation so that others could re-create your results.** Therefore, simply add to this document to arrive at your lab report, as all of the explanatory text, procedures and Discussion and Conclusion questions contained in this document are required for a complete lab report. So for your lab report, **add a cover page, your results, along with your answers to the Discussion and Conclusions questions to the existing lab document**. Your answers to the **Discussion and Conclusions** questions are to **be uniquely yours** and not a copy of someone else’s answers to these questions. Your cover page is to include class, lab title, and author. A grading rubric for this lab is included at the end of this document. The rubric does not need to be included in your lab report.

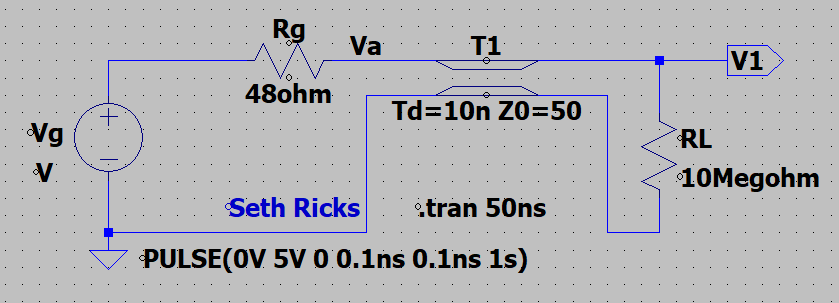
**Purpose:** To better understand Waveform Reflections for Pulsed Waveforms on Transmission Lines, along with Time Domain Reflectometry, i.e., TDR.

**Procedure:**

**Part 1 – Open, Shorted and Terminated Transmission Lines**

Note: There is something buggy about the LTspice **tline** component at the load end of the line, that can result in a load voltage Vl equal to zero, when it should not be zero. Consequently, placing the load resistor Rl after placing the **tline** component is recommended during circuit construction. If your circuit has load voltage Vl always equal to zero even with the desired signal applied, try deleting then replacing load resistor Rl.

1. Construct the circuit shown below in **Figure 1** in LTspice. **The PULSE statement is to be added by right clicking on the voltage source and choosing PULSE as the function, then entering the associated values for Vinitial(V): Von(V):, Tdelay(s): Trise(s):, Tfall(s): and Ton(s):. Adding the PULSE statement as a Spice Directive does not associate the PULSE with the voltage source.** Add the Net Names **Va** and **Vl**, to readily plot those voltages in the plot pane. Note: Rg is to be set at 48 Ω, instead of the ideal 50 Ω to provide slight ongoing reflections as observed when working with practical measurement systems. Configure the simulation to do a transient analysis of duration 50ns. In the **Edit** pull-down menu, add your name to your schematic as follows: **Edit 🡪 Aa Text**.
2. When completed with your schematic, replace the schematic shown in **Figure 1** below with your version, including your name. (7 points.)

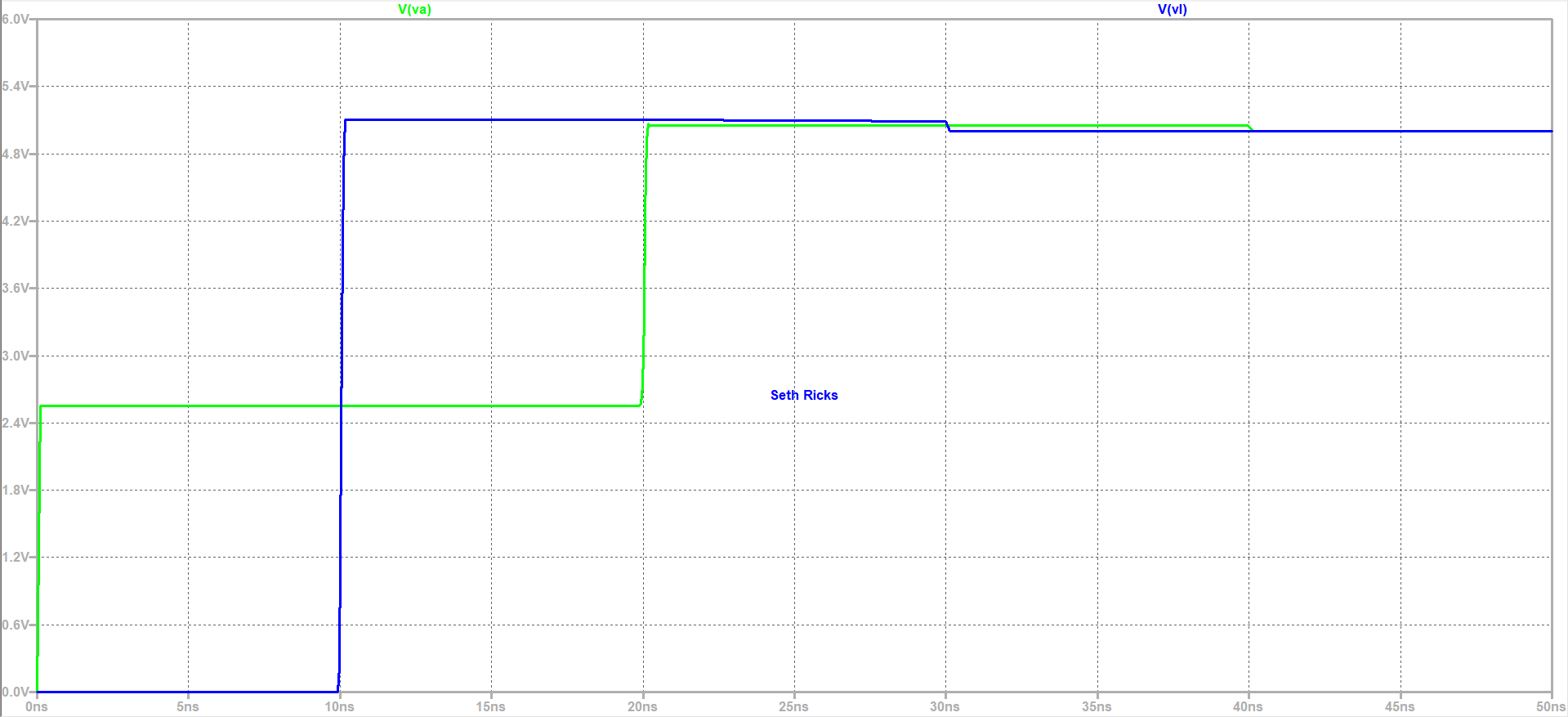


**Figure 1:** Simulation Circuit for an Open Transmission Line.

1. After running the simulation, a Plot Pane will open in which you are to select the waveforms **V(va)** and **V(vl)** for display.

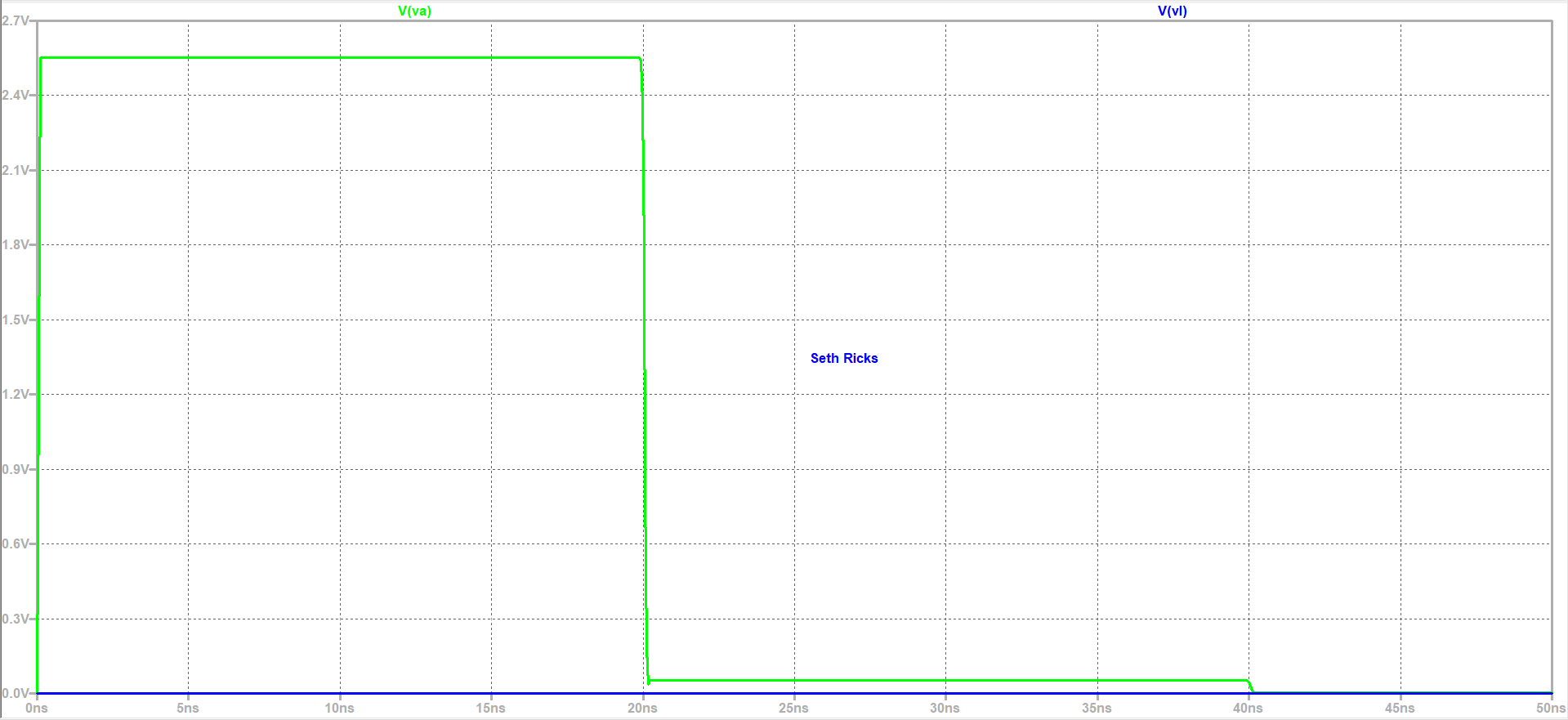
Note: LTspice uses a dark background for the default plot pane, which makes it hard to visibly see some trace colors such as dark blue. The **Tools** 🡪 **Control Panel** 🡪 **Waveforms** 🡪 **Color Scheme** 🡪 **Background** allows you to modify the background color with Red = Green = Blue = 255 resulting in a white background. This is an optional change that you may find improves waveform viewing. If you make this change, it is also recommended to navigate to **Tools** 🡪 **Control Panel** 🡪 **Waveforms** and change the **Data Trace** and **Cursor width** from 2 to 3, along with using a Bold Font for the waveform labels so that the traces, cursors are waveform labels are more easily visualized.

1. In the Plot Settings pull-down menu on the main LTspice toolbar, annotate your plot with your name as follows: **Plot Settings 🡪 Notes & Annotations 🡪 Place Text**.
2. Replace the plot pane in **Figure 2** below with your version. (3 points.)

****

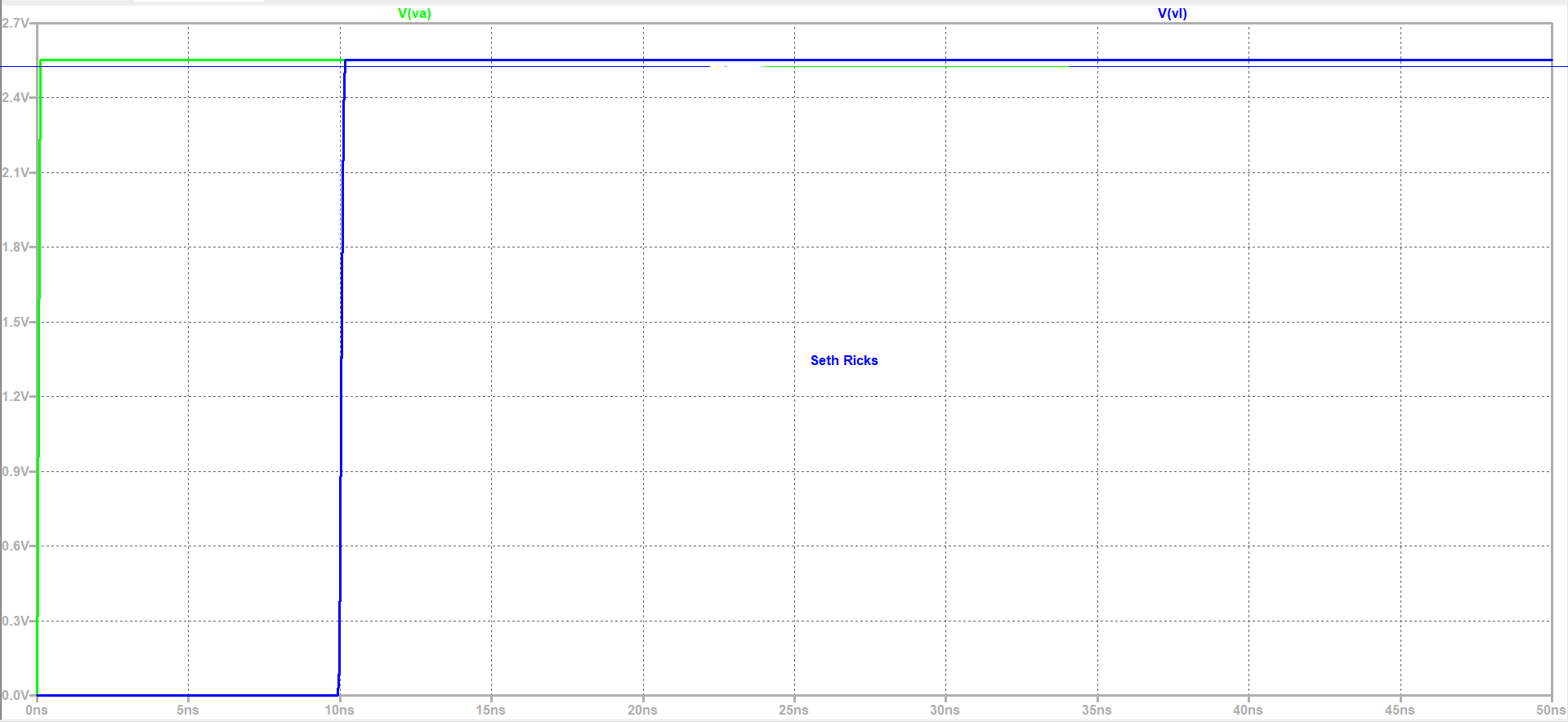
**Figure 2:** Simulated Results for the Open Transmission Line Circuit of **Figure 1**.

1. Next modify your **Figure 1** circuit from an open to a shorted transmission line, by changing Rl from 10M Ω to 0.01 Ω and re-run the simulation.
2. After running the simulation, a Plot Pane will open in which you are to select the waveforms **V(va)** and **V(vl)** for display.
3. In the Plot Settings pull-down menu on the main LTspice toolbar, annotate your plot with your name as follows: **Plot Settings 🡪 Notes & Annotations 🡪 Place Text**.
4. Replace the plot pane in **Figure 3** below with your version. (3 points.)



**Figure 3:** Simulated Results for a Shorted Transmission Line.

1. Next modify your **Figure 1** circuit from an open to a terminated transmission line, by changing Rl to 50 Ω and re-run the simulation.
2. After running the simulation, a Plot Pane will open in which you are to select the waveforms **V(va)** and **V(vl)** for display.
3. In the Plot Settings pull-down menu on the main LTspice toolbar, annotate your plot with your name as follows: **Plot Settings 🡪 Notes & Annotations 🡪 Place Text**.
4. Replace the plot pane in **Figure 4** below with your version. (3 points.)

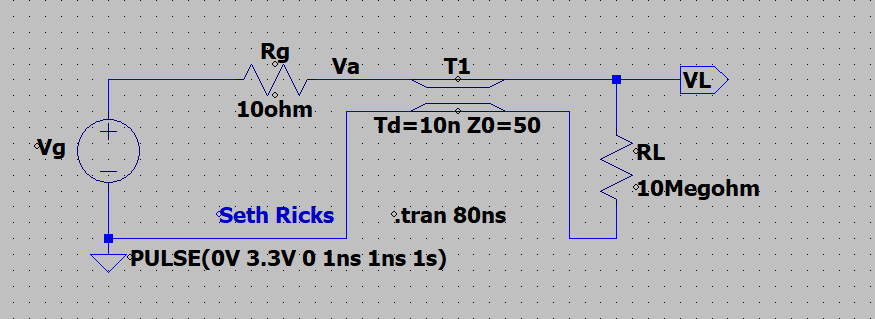


**Figure 4:** Simulated Results for a 50 Ω Terminated Transmission Line.

**Part 2 – Digital Circuits and Waveform Reflections**

Most modern digital logic circuits consist of high-speed digital outputs connected to high input-impedance digital inputs, forming an open transmission line. Consequently, digital logic circuits having fast rise and fall times can suffer from logic level corruption due to waveform reflections. Hence, high-speed digital logic designers need to understand transmission lines.

1. Construct the circuit shown below in **Figure 5** in LTspice. Add the Net Names **Va** and **Vl**, to readily plot those voltages in the plot pane. Configure the simulation to do a transient analysis of duration 80 ns. In the **Edit** pull-down menu, add your name to your schematic as follows: **Edit 🡪 Aa Text**.
2. When completed with your schematic, replace the schematic shown in **Figure 5** below with your version, including your name. (6 points.)



**Figure 5:** Simulation Circuit for an Unterminated Digital Logic Circuit.

A Bounce Diagram, like the one illustrated below in **Figure 6**, is to be used to determine the step response of the **Figure 5** circuit at both the generator and load end of the transmission line. As indicated in **Figure 6**, several calculated values are necessary to complete the Bounce Diagram. In **Figure 6**, the first reflected component occurs at time = 10 ns, after which all additional traces are due to reflections from either the load end or generator end. The larger the magnitude of each of these reflections, the larger the magnitude of the associated voltage changes at the load or generator end of the transmission line.

A close up of a map

Description automatically generated

**Figure 6:** Generic Bounce Diagram for a Transmission Line Circuit Having a 10 ns Propagation Delay.

1. Given that Vg generates 0 V to 3.3 V step starting at 0 ns in the circuit of **Figure 5**, calculate all the values indicated below in **Table 1**, which are necessary to complete the Bounce Diagram corresponding to the first 80 ns of the applied step. Use at least 4 significant figures in your calculations and include units where appropriate.

(10 points total.)

**Table 1**: Calculated Values Needed to Complete the Bounce Diagram for the **Figure 5** Circuit.

|  |  |
| --- | --- |
| Bounce Diagram Parameter | Calculated Value with Units where Appropriate |
|  | 2.750 V |
|  | -0.6667 |
|  | 0.99999 |
|  | 2.74997 V |
|  | -1.8333 V |
|  | -1.8332967 V |
|  | 1.2221978 V |
|  | 1.22219 V |
|  | -0.81479 V |
|  | -0.814782 V |

Next using at least 4 significant figures, determine the voltages at both the generator and load end of the transmission lines for each time listed in **Table 2** below. Determining these voltages is best accomplished by utilizing a Bounce Diagram annotated with your calculated values from **Table 1**. A Bounce Diagram without voltage values is included below in **Figure 7**, as an aid to determining your calculated **Table 2** values. The Bounce Diagram of **Figure 7** is only an aid in your calculations, with no points awarded to the Bounce Diagram, instead points are awarded for correctly calculated **Table 1** and **Table 2** values. To determine voltage versus time at the generator end of the transmission line, i.e., Va, traverse the bounce diagram downward along the left-hand vertical edge that corresponds to z = 0, and then algebraically add up the voltages associated with the zig-zag bounces. To determine the voltage versus time at the load end of the transmission line, i.e., Vl, traverse the bounce diagram downward along the right-hand vertical edge that corresponds to z = l, and then algebraically add up the voltages associated with the zig-zag bounces. Your calculated response is then to be compared with the LTspice simulation results, also to be included in **Table 2** below. (16 points total.)

A picture containing sitting

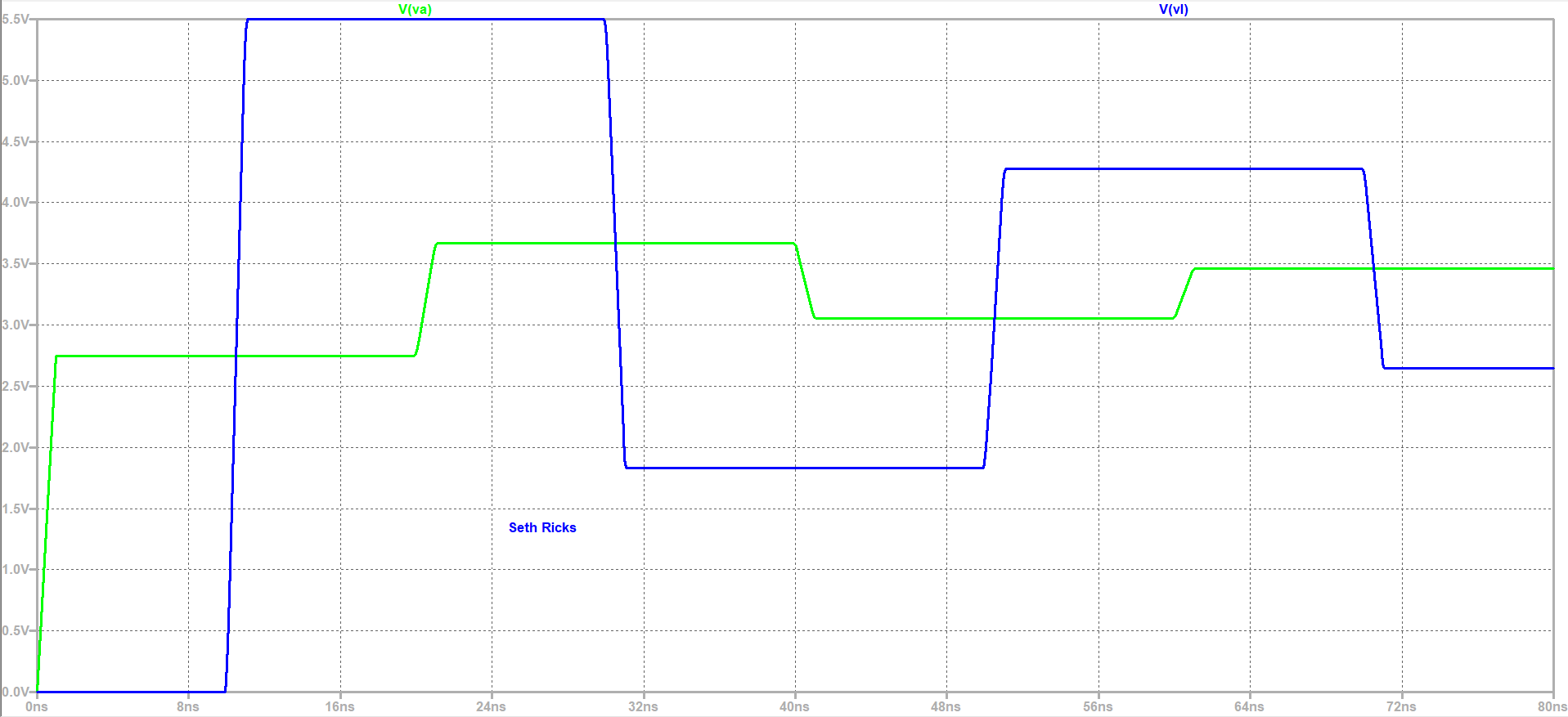
Description automatically generated

**Figure 7:** Bounce Diagram for the Digital Logic Circuit of **Figure 5**.

**Table 2**: Calculated and Simulated Va and Vl Voltages versus Time for the Circuit of **Figure 5**.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Time | Va\_calculation | Vl\_calculation | V(va)\_simulation | V(vl)\_simulation |
| 5 ns | 2.750 V | 0.000 V | 2.750 V | 0.000 V |
| 15 ns | 2.750 V | 5.49997 V | 2.750 V | 5.4999857 V |
| 25 ns | 3.66666575 V | 5.49997 V | 3.6666574 V | 5.4999857 V |
| 35 ns | 3.66666575 V | 1.833361 V | 3.6666574 V | 1.8333619 V |
| 45 ns | 3.055559 V | 1.833361 V | 3.0555587 V | 1.8333619 V |
| 55 ns | 3.055559 V | 4.2777442 V | 3.0555587 V | 4.2777467 V |
| 65 ns | 3.462954 V | 4.2777442 V | 3.4629538 V | 4.2777467 V |
| 75 ns | 3.462954 V | 2.6481716 V | 3.4629538 V | 2.6481731 V |

1. Next run the LTspice simulation for the circuit of **Figure 5**.
2. After running the simulation, a Plot Pane will open in which you are to select the waveforms **V(va)** and **V(vl)** for display.
3. In the Plot Settings pull-down menu on the main LTspice toolbar, annotate your plot with your name as follows: **Plot Settings 🡪 Notes & Annotations 🡪 Place Text**.
4. Replace the plot pane in **Figure 8** below with your version. (3 points.)



**Figure 8:** Simulated Results for an Unterminated Digital Logic Circuit.

1. Next using cursors, determine the simulated voltages versus time at the generator, i.e., Va, and the load, i.e., Vl, and enter those values in **Table 2** located above as simulated values. Note: Your calculated and simulated **Table 2** values should closely agree, or else something is amiss with either your calculations, or simulations or both.

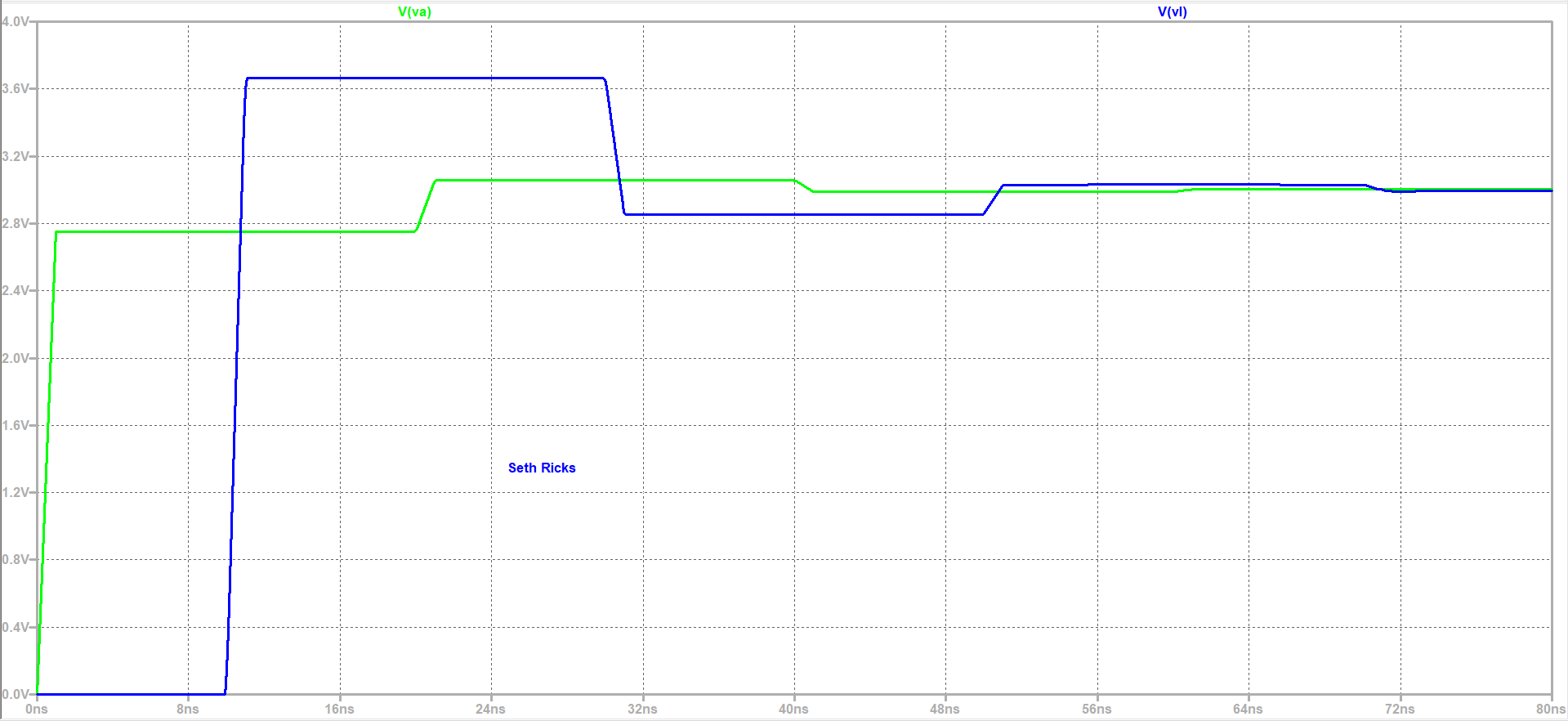
The step response waveform shown above in **Figure 8** is unacceptable for digital systems, as the waveform ringing would result in mis-interpreted logic levels. Yet exact matching of the generator, transmission line characteristic impedance and load impedance is burdensome and not necessary for high-speed digital systems. Instead a fairly simple remedy is to terminate the line at **Vl** with a 100 Ω or smaller resistor, which results in good enough behavior for digital systems. Since the smaller the value of the termination resistor, the larger the current consumption for a digital “1” value applied across the termination resistor, the largest resistance value that results in acceptable behavior is often chosen for termination resistors.

1. Modify your **Figure 5** circuit from an open to a terminated transmission line, by changing Rl from 10MΩ to 100 Ω, which changes .
2. Re-calculate the bounce diagram parameters from **Table 1** as needed starting with , to complete **Table 3** below, for the circuit of **Figure 5** with a 100 Ω load resistor. Use at least 4 significant figures in your calculations and include units where appropriate. Note: Your calculated component should be approximately -10 mV. (8 points.)

**Table 3**: Calculated Values Needed to Complete the Bounce Diagram for the **Figure 5** Circuit with a 100 Ω Load Resistor.

|  |  |
| --- | --- |
| Bounce Diagram Parameter | Calculated Value with Units where Appropriate |
|  | 2.750 V |
|  | -0.6667 |
|  | 0.333 |
|  | 0.91667 V |
|  | -0.6111 V |
|  | -0.2037 V |
|  | 0.1358 V |
|  | 0.0453 V |
|  | -0.0302 V |
|  | -0.0101 V |

1. Re-run your LTspice simulation, after which a Plot Pane will open in which you are to select the waveforms **V(va)** and **V(vl)** for display.
2. In the Plot Settings pull-down menu on the main LTspice toolbar, annotate your plot with your name as follows: **Plot Settings 🡪 Notes & Annotations 🡪 Place Text**.
3. Replace the plot pane in **Figure 9** below with your version. (3 points.)



**Figure 9:** Simulated Results for a Terminated Digital Logic Circuit.

**Part 3 – Time Domain Reflectometry**

Problems can become opportunities. TDR (Time Domain Reflectometry) utilizes reflections associated with impedance mismatches to characterize wave propagation (phase) velocity or length of a transmission line. When a fast rise-time step in voltage is applied to a transmission line a transient wave propagates along the transmission line to the load. If the impedance of the load differs from the characteristic impedance of the transmission line then a reflected waveform travels from the load back to the source. By monitoring the transmission line voltage at the generator end, the time for the down and back wave propagation along the line can be viewed. If the length of the transmission line is known, then the wave propagation (phase) velocity can be calculated, whereas if the wave propagation (phase) velocity is known, then the length of the line can be calculated. This technique is used to locate faults along buried transmission lines, along with other applications including soil moisture measurements where the presence of liquid water slows the propagation (phase) velocity of a transient wave applied to metal rods buried in the soil.

For a fast rise-time step propagation along a transmission line, the relationship between line length L, wave propagation (phase) velocity up, and two-way transmission line propagation time tp is given as follows:

For coaxial cable transmission lines up typically ranges between 0.6c to 0.7c, where c is the speed of light, i.e.,

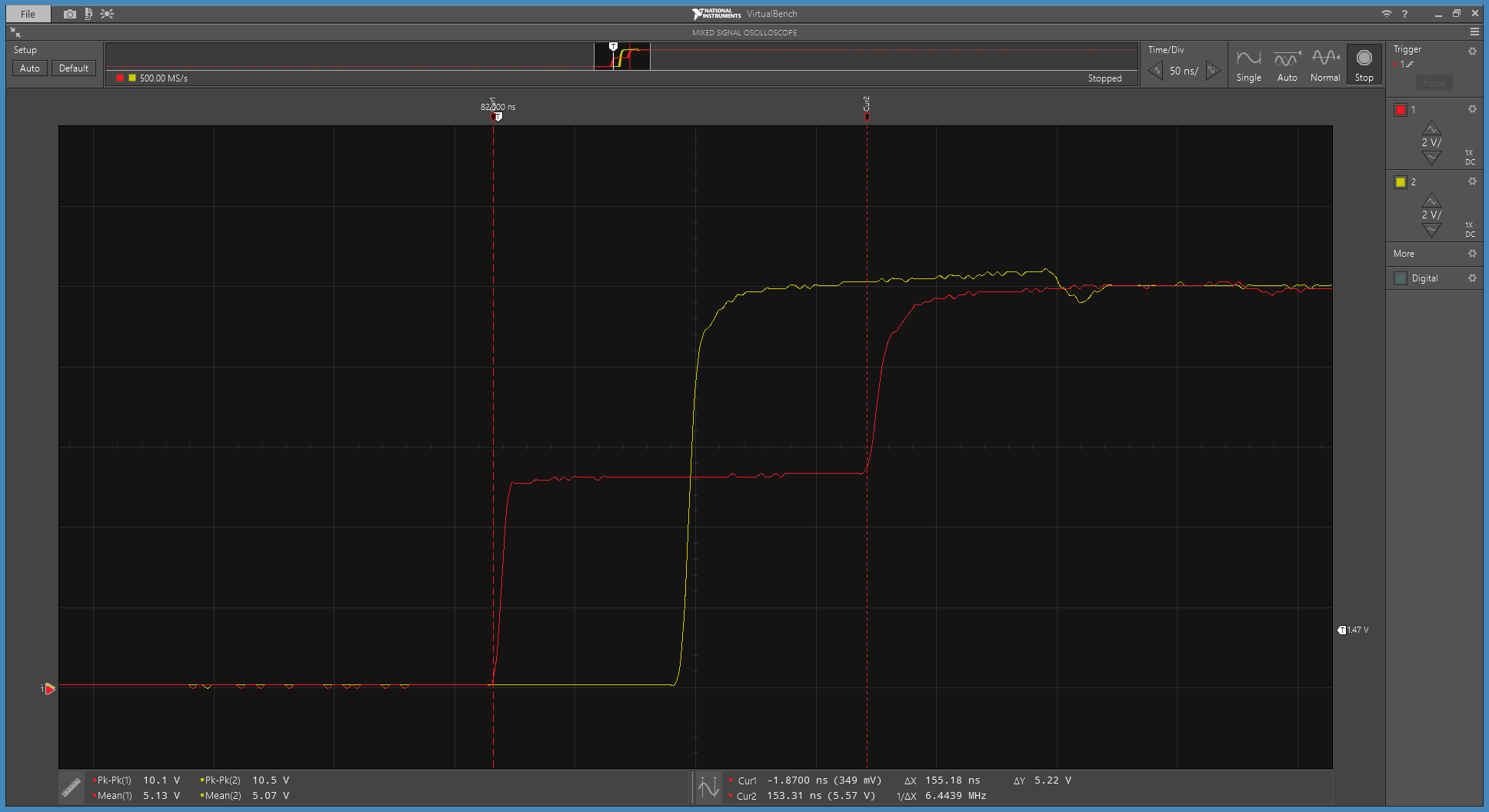
For cables longer than a few feet, a function generator and oscilloscope can be used to measure either the propagation velocity up, or the length of the cable. For the following portion of the lab a VirtualBench measurement system was used to measure the propagation velocity up of a 50 foot 50 Ω RG58A coaxial cable using the configuration shown below in **Figure 10**.



**Figure 10**: Set-up for TDR Measurement Using a Function Generator and Oscilloscope.

In the above setup, the VirtualBench function generator produces a 0 to 10 V, 100 Hz square wave, which is connected to Channel 1 of the oscilloscope along with the cable to be tested. The end of that cable is then connected into Channel 2 of the oscilloscope, providing for waveform viewing at both ends of the cable.

The setup illustrated in Figure 9 was used to characterize a 50 foot 50 Ω RG58A coaxial cable, with the results shown below in **Figure 11**.



**Figure 11**: Transient Response to a Step Input for a 50 Foot Open-Ended Transmission Line.

As can be seen, from the cursors in **Figure 11**, a total two-way propagation time of tp = 155 ns was measured for the 50 foot 50 Ω RG58A coaxial cable. Note: The time tp is the two-way propagation time and therefore equals 2td, where td is the one-way propagation time.

1. Calculate the wave propagation (phase) velocity in units of meters per second for the 50 foot 50 Ω RG58A coax cable, including at least two steps of your work. Record your calculated value including units below: (3 points total, 2 points for at least two steps of work shown, 1 point for correct answer.)

up for 50 foot 50 Ω RG58A coax cable:

**Discussion and Conclusions Questions:** (For the following questions use your own words along with complete sentences. Answer your questions so that readers can understand your response without having to read the question.)

1. For an ideal open-ended transmission line having a 50 Ω generator and characteristic impedance, describe the major wave propagation events up to the return of the first reflection to the generator at time 2td. These events are displayed in **Figure 2**, except for Rg = 48 Ω rather than 50 Ω in **Figure 2**. Start your description with the launching of a fast rise-time step from a function generator with a 50 Ω output (generator) impedance connected to the input of an open-ended 50 Ω transmission line. Include the voltage levels of the incident and reflected waveforms in your description. (4 points.)

This situation means that there is an open at the end of the transmission line, which results in a reflection coefficient of 1, with no phase shift. The load is perfectly mismatched from the characteristic impedance. By contrast, the generative impedance is perfectly matched to the characteristic impedance. When the wave leaves the generator, all the generator sees is the characteristic impedance. The initial voltage leaving the generator will be a voltage divider of the characteristic impedance and the generative impedance. When the wave reaches the load, or in this case an open, the reflection has the same magnitude and phase as the original wave. When the wave reaches the generator again, it sees a voltage of twice the original voltage. There are no reflections afterwards, because of the perfectly matched generator resistance to the characteristic impedance.

1. For an ideal shorted transmission line having a 50 Ω generator and characteristic impedance, describe the major wave propagation events up to the return of the first reflection to the generator at time 2td. These events are displayed in **Figure 3**, except for Rg = 48 Ω rather than 50 Ω in **Figure 3**. Start your description with the launching of a fast rise-time step from a function generator with a 50 Ω output (generator) impedance connected to the input of a shorted 50 Ω transmission line. Include the voltage levels of the incident and reflected waveforms in your description. (4 points.)

This situation is very similar to think about as the open transmission line. The only difference is that now we are dealing with a short, so the reflection coefficient will have a magnitude of 1 with a phase shift of 180 degrees. The generator and characteristic impedance are still matched. The initial voltage wave leaving the generator will still be a voltage divider of the characteristic impedance and the generative impedance. When the wave reads the load, or the short, the reflection with have the same magnitude as the original voltage, and the opposite phase. This means that that the voltage leaving the load will be 0V net. This is what the generator will then see. There are no further reflections, because of the matched generator resistance to the characteristic impedance.

1. Explain how changing the load resistance from 10MΩ to 100 Ω in the **Figure 5** circuit of **Part 2** reduced the signal reflections to an acceptable level for digital signals. (2 points.)

Switching the load resistance from 10MΩ to 100Ω resulted in a more closely matched load. This was because the characteristic impedance was 50Ω, which is way closer to 100Ω than to 10MΩ. When the load is closer to the load resistance, the reflection coefficient is closer to 0, meaning that there are smaller reflections.

1. For your calculated wave propagation (phase) velocity in units of meters per second for the 50 foot 50 Ω RG58A coax cable in **Part 3**, determine the wave propagation (phase) velocity in terms of a decimal fraction times the speed of light, i.e., kc, where k < 1 and c = (2 points.)

**LTspice TDR Lab Grading Rubric:** **This is a CAD lab to be done individually, rather than in teams, although please help each other out if/when opportunities arise, avoiding plagiarism. Submit an electronic version of a lab report to receive credit for doing this lab.** The goal of your **lab report is to provide sufficient documentation so that others could re-create your results.** Therefore, simply add to this document to arrive at your lab report, as all of the explanatory text, procedures and Discussion and Conclusion questions contained in this document are required for a complete lab report. So for your lab report, **add a cover page, your results, along with your answers to the Discussion and Conclusions questions to the existing lab document**. Your answers to the **Discussion and Conclusions** questions are to **be uniquely yours** and not a copy of someone else’s answers to these questions. Your cover page is to include class, lab title, and author. The rubric below does not need to be included in your lab report.

|  |  |
| --- | --- |
| **Lab Report Item** | **Points** |
| Cover Page | 1 |
| **Part 1** **– Open, Shorted and Terminated Transmission Lines**  **Figure 1**: (7 points total. 1 point for voltage source with **PULSE(0V 5V 0 0.1ns 0.1ns 1s)** configuration statement, 1 point for Rg, 1 point for Rload, 2 points for T1 along with Td = 10ns and Zo = 50Ω, 1 point for **.tran 50ns** statement, 1 point for name included on schematic.)  **Figure 2**: (3 points total. 1 point for **V(va)** trace, 1 point for **V(vl)** trace, 1 point name included on the plot pane.)  **Figure 3**: (3 points total. 1 point for **V(va)** trace, 1 point for **V(vl)** trace, 1 point name included on the plot pane.)  **Figure 4**: (3 points total. 1 point for **V(va)** trace, 1 point for **V(vl)** trace, 1 point name included on the plot pane.) | 16 |
| **Part 2 – Digital Circuits and Waveform Reflections**  **Figure 5**: (6 points total. 1 point for voltage source with **PULSE(0V 3.3V 0 1ns 1ns 1s)** configuration statement, 1 point for Rg, 1 point for Rload, 1 point for T1 along with Td = 10ns and Zo = 50Ω, 1 point for **.tran 80ns** statement, 1 point for name included on schematic.)  **Table 1**: (10 points total. 1 point per entry. -0.25 points per missing or incorrect units.)  **Figure 8**: (3 points total. 1 point for **V(va)** trace, 1 point for **V(vl)** trace, 1 point name included on the plot pane.)  **Table 2**: (16 points total. 0.5 points per entry. -0.1 points per missing unit.)  **Table 3**: (8 points total. 1 point per entry. -0.25 points per missing or incorrect units.)  **Figure 9**: (3 points total. 1 point for **V(va)** trace, 1 point for **V(vl)** trace, 1 point name included on the plot pane.) | 46 |
| **Part 3 – Time Domain Reflectometry**  Calculated up for 75 foot 50 Ω RG58A coax cable. (3 points, with 1 point for correct answer.) | 3 |
| Discussion and Conclusions | 12 |
| Grammar and Professionalism | 4 |
|  |  |
| **Total** | 82 |

Please give feedback on errors you find in this document.